PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER WITH TWO-POINT MODULATION

ABSTRACT OF THE DISCLOSURE

A phase-locked loop (PLL) frequency synthesizer having a two-point data modulation scheme and $\Sigma\Delta$ modulator, fractional-N architecture. In the synthesizer, data are modulated at both the PLL frequency divider and the voltage-controlled oscillator (VCO). The complementary frequency responses at these two modulation points allow the PLL bandwidth to be sufficiently narrow to attenuate phase noise from the phase detector, frequency divider, and $\Sigma\Delta$ quantization error, without adversely affecting the data. Fractional-N architecture allows a large range of reference frequencies to be used with the PLL and high frequency resolution of the output signal. The $\Sigma\Delta$ modulator modulates the feedback signal generated by the PLL frequency divider with data and quantizes the spurious signals inherent in a fractional-N design to high frequencies that the PLL loop filter can attenuate.